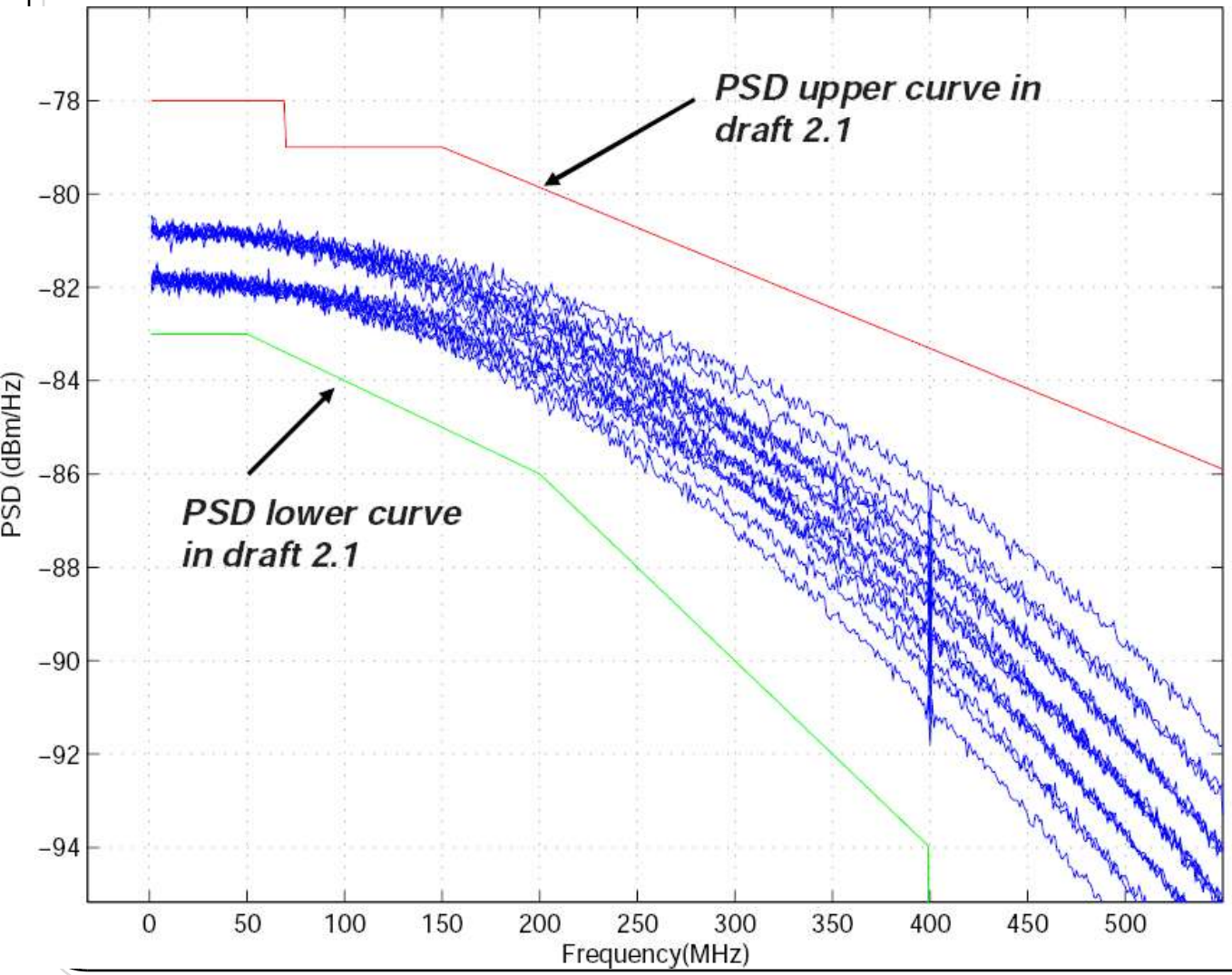
Study of 10GBase-T Transmitter

指導教授：汪重光
學生：葉治億

- Survy on IEEE 802.3an task force material
- The impairment of the DAC
- Random walk method
- Dynamic random walk
- Working Items

PSD Specification

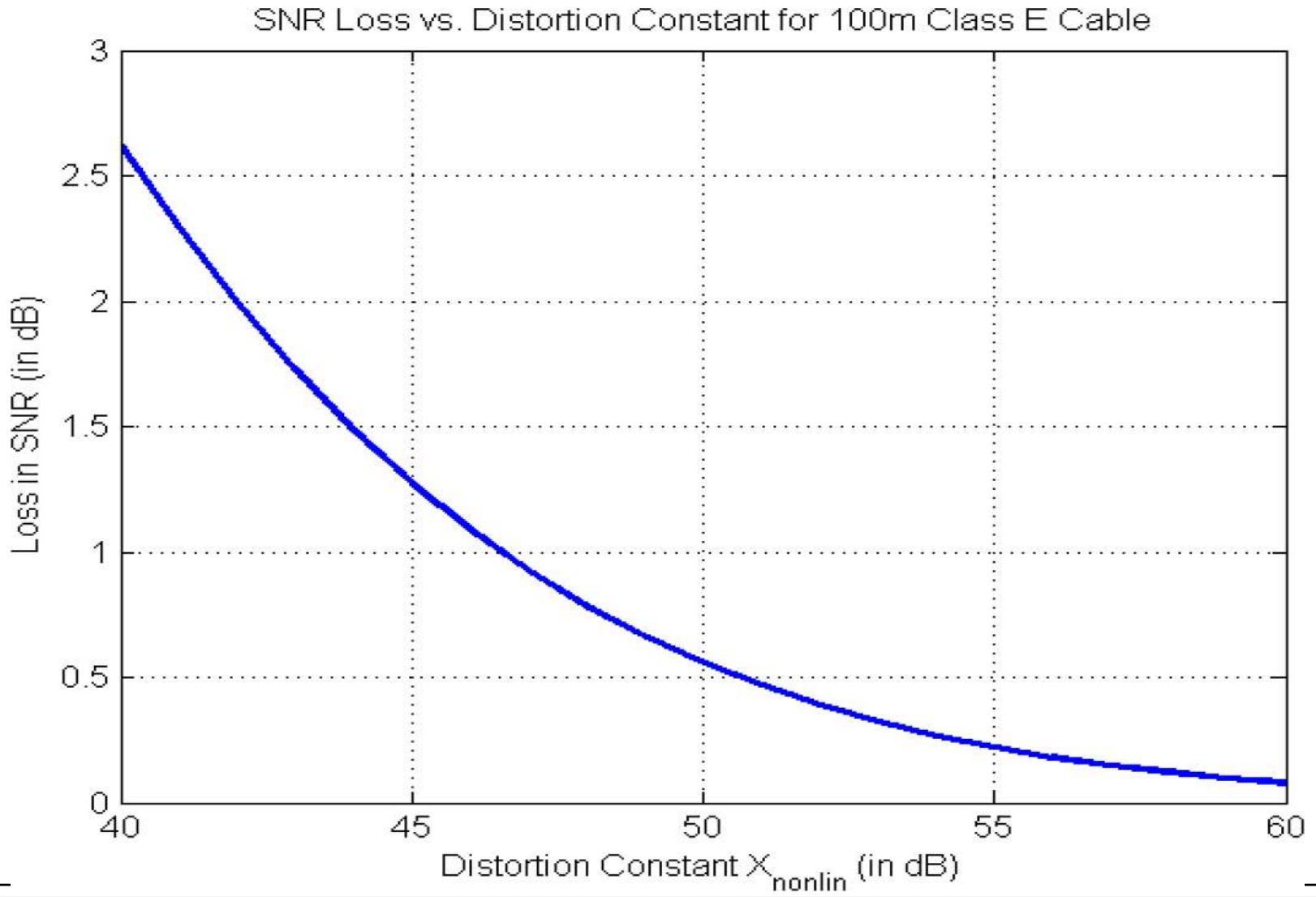


Note:

- *With 2V +/- 6% at the transformer output, the lower PSD curve has smaller margin at lower end.*
- *2V +/- 6% with the filter tolerances as specified meets the power spec*
- *Upper PSD has a larger margin, especially the lower 0-70MHz range.*

[Sandeep Gupta and Ramin Shirani, "10GBASE-T Transmitter PSD", July 2005 Plenary week material in IEEE 802.3an Task Force]

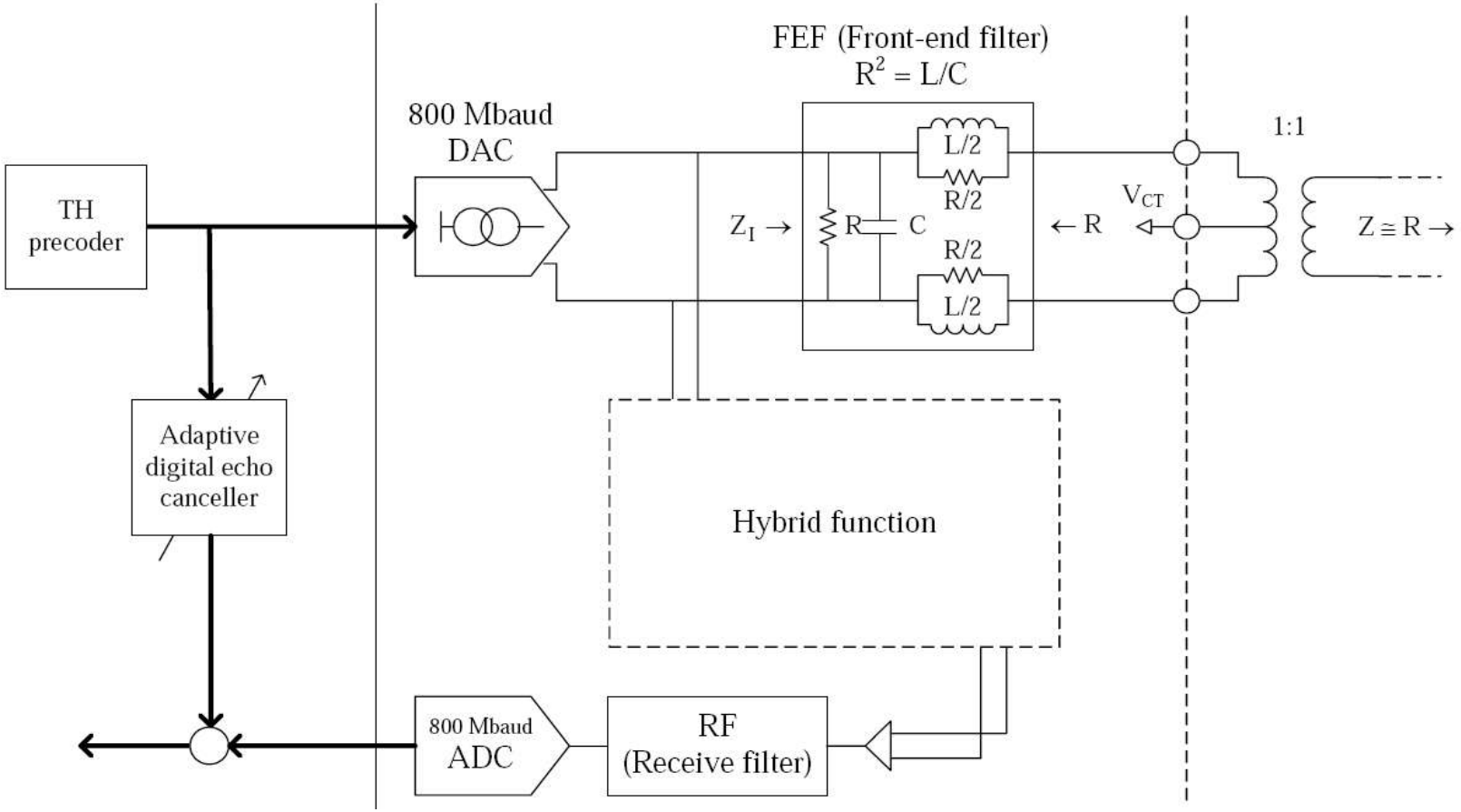
Nonlinear Distortion



[Bijit Halder, "Effect of Transmit Distortion On Receiver SNR", February 2005 Interim Meeting of IEEE 802.3an Task Force]

Transmitter from Broadcom (I)

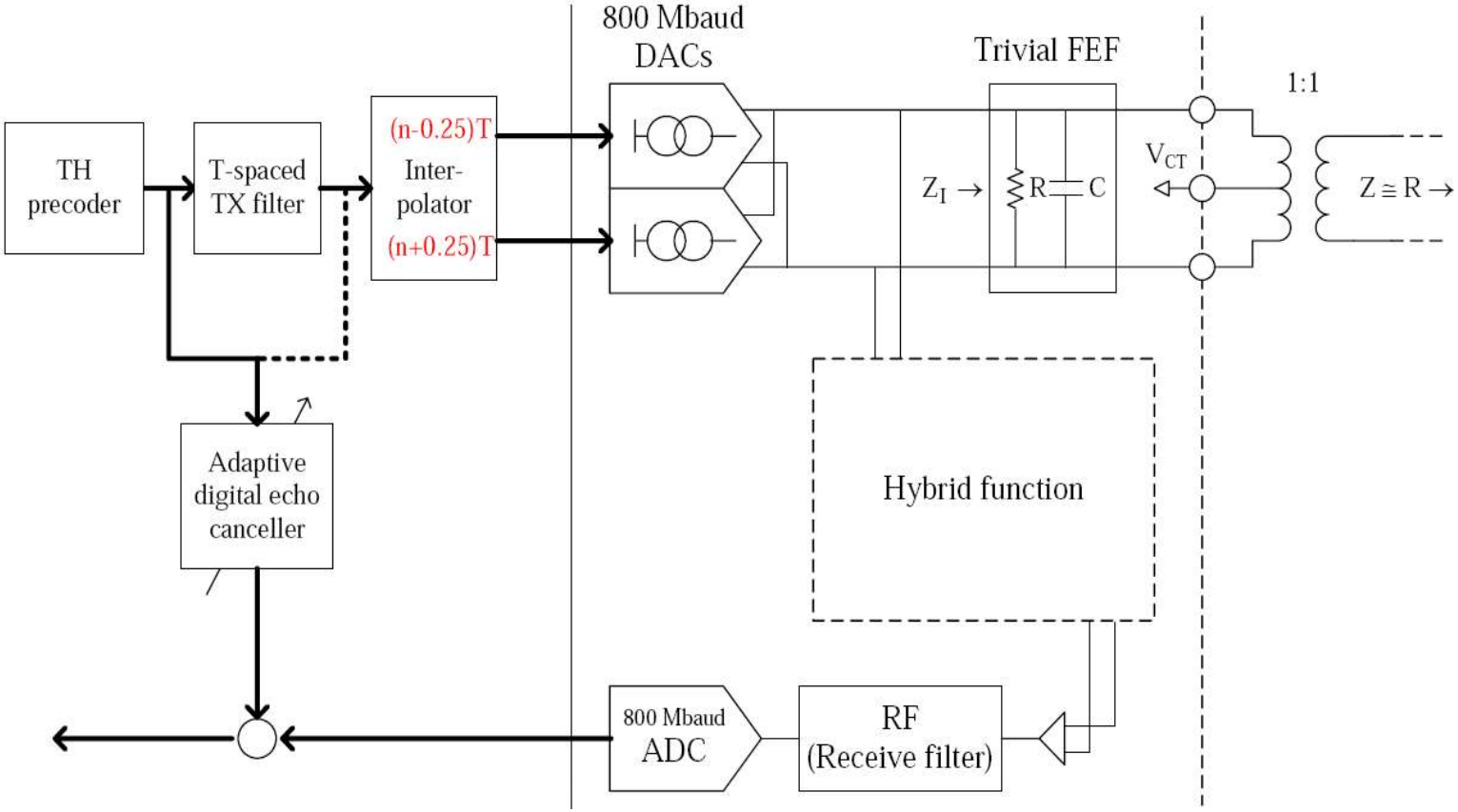
No digital filtering, T-spaced DAC, front-end filter with frequency-dependent input impedance Z_I and constant output impedance R



[Gottfried Ungerboeck and Scott Powell, "10GBASE-T Cable characteristics, front-end solutions, and precoders", IEEE P802.3an Task Force, Atlanta, March 22-24, 2005]

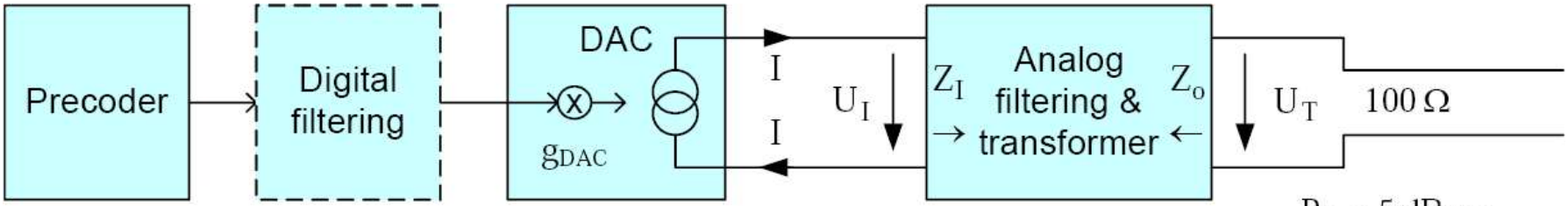
Transmitter from Broadcom (II)

Digital TX-filtering & T/2-interpolation, T/2-overlapping DACs, trivial front-end filter



[Gottfried Ungerboeck and Scott Powell, "10GBASE-T Cable characteristics, front-end solutions, and precoders", IEEE P802.3an Task Force, Atlanta, March 22-24, 2005]

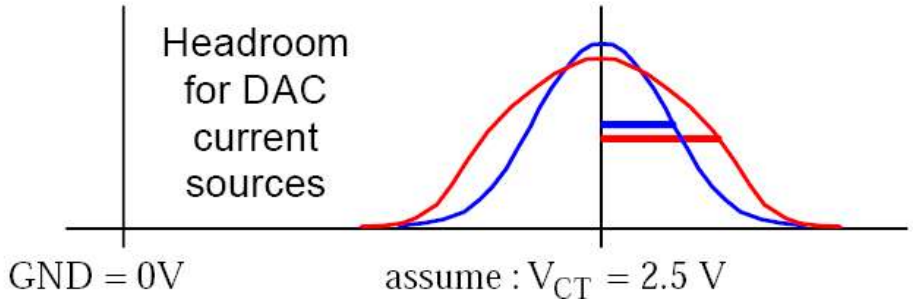
Transmitter from Broadcom (III)



$P_T = 5$ dBm :
$U_T = 562.3\ mV_{rms}$

Baseline approach : $I = 15.9\ mA_{rms},\ U_I = 891.1\ mV_{rms,diff} \triangleq V_{CT} \pm 445 mV_{rms}$

Preferred appraoch : $I = 12.7\ mA_{rms},\ U_I = 630.7\ mV_{rms,diff} \triangleq V_{CT} \pm 315.3 mV_{rms}$



Preferred approach has lower (-3 dB) rms-voltage at DAC outputs than baseline approach, but (presumably) higher peak-to-average ratio.

[Gottfried Ungerboeck and Scott Powell, "10GBASE-T Cable characteristics, front-end solutions, and precoders", IEEE P802.3an Task Force, Atlanta, March 22-24, 2005]

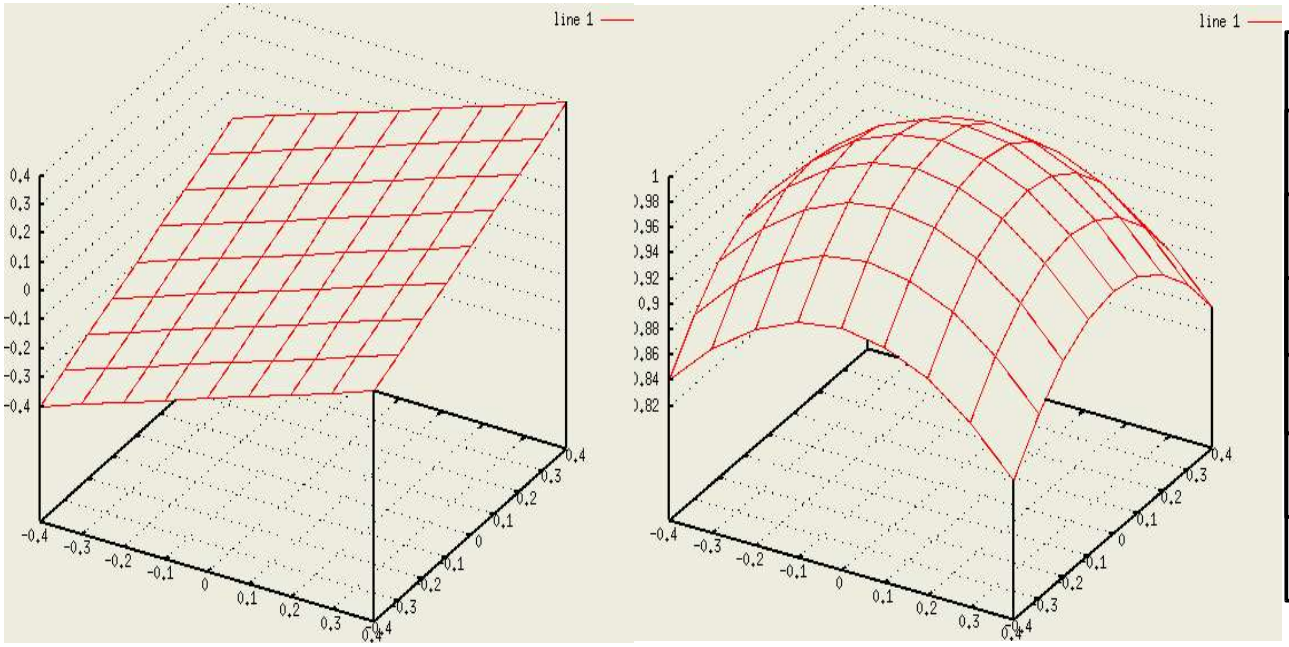
The Impairment of the DAC

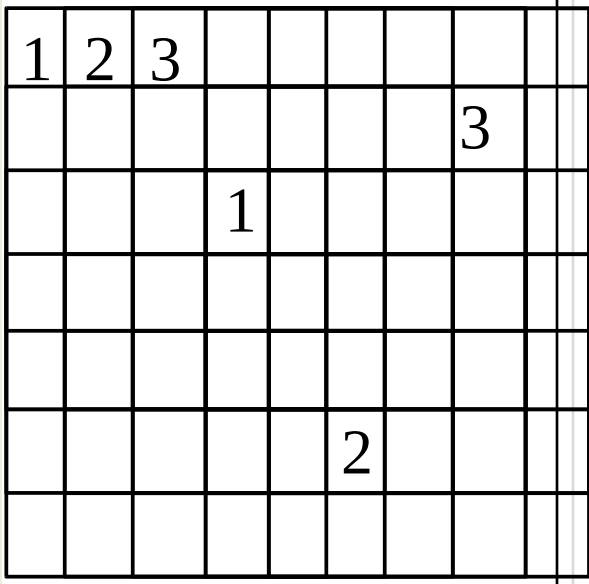
- DC accuracy
  - Random errors: device mismatches
  - Systemic errors:
    - Linear gradient: common centroid
    - Higher order effects
- AC accuracy
  - Voltage Fluctuation
  - Control signals feedthrough
  - Clock synchronization

[Jose Bastos et al, "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC", IEEE J. Solid-State Circuits, Vol. 33, No. 12 Dec. 1998]

Random Walk Method

- Use random walk method to mitigate systemic mismatch

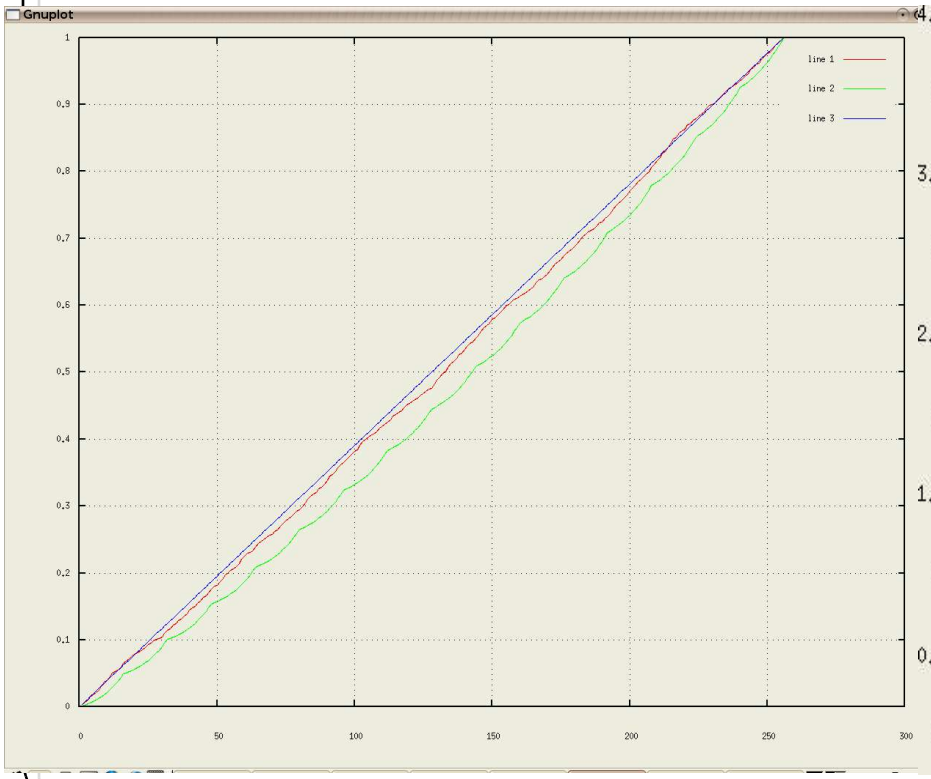


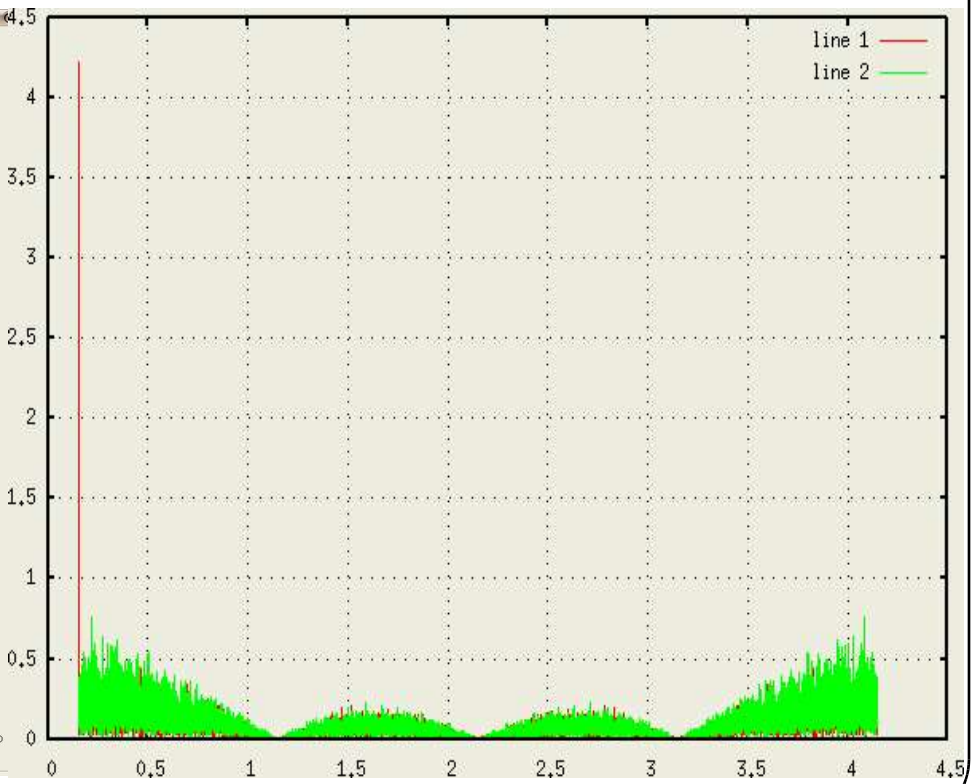


[Geert A. M. et al, "A 14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC", IEEE JSSC Vol. 34, No. 12, Dec. 1999]

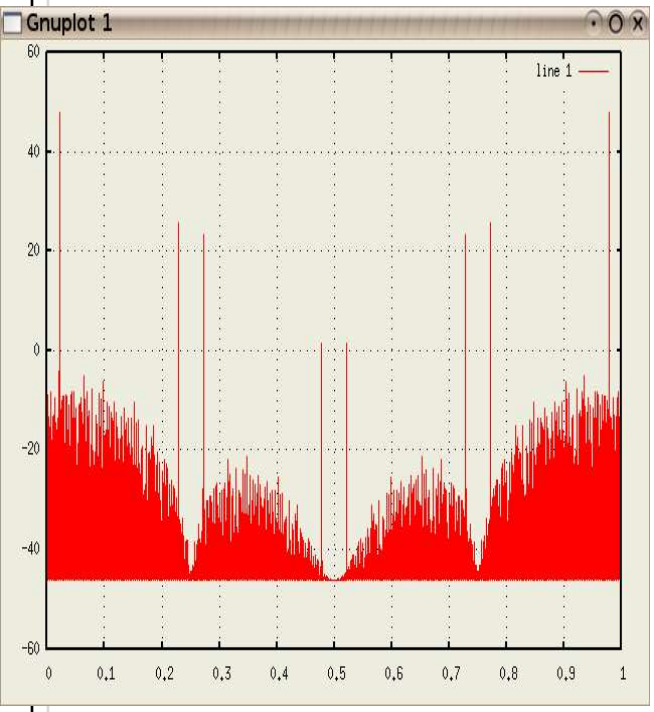
Dynamic Random Work

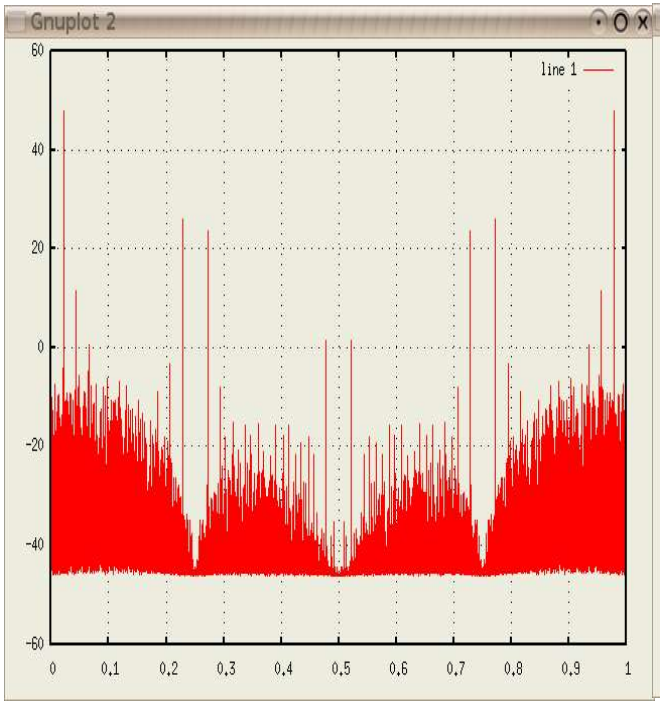
- Use switch as round robin

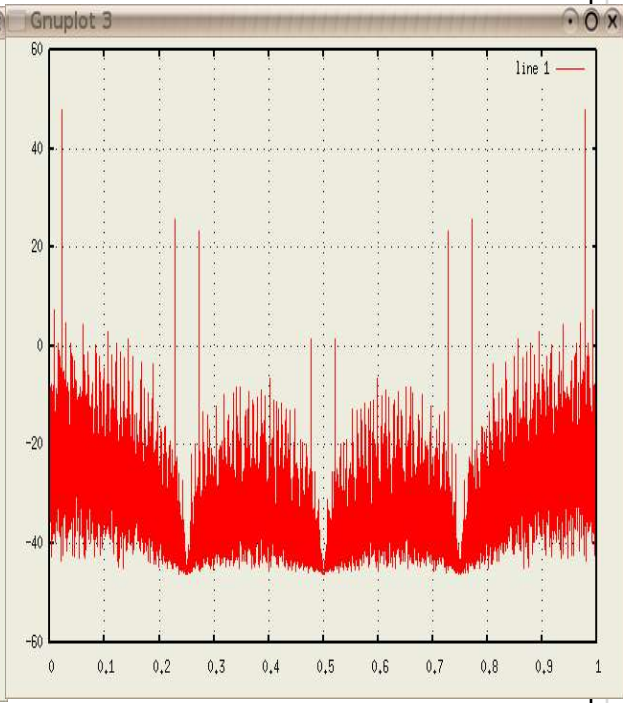




Spur in the Sine Wave Simulation







Working Items

10Gbase-T Transmitter

- ☑Transmitter architecture design
- ☑DAC design
  - ☑System design
  - ☐Circuits design
  - ☐Layout and verification
- ☐Line driver design
  - ☐System design
  - ☐Circuits design
  - ☐Layout and verification
- ☐Hybrid design
  - ☐System design
  - ☐Circuits design
  - ☐Layout and verification

■Finished ☑On-going ☐Future work